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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,597	04/12/2005	Seung-Hee Yu	YOM-0100	9540
23413	7590	10/10/2008	EXAMINER	
CANTOR COLBURN, LLP			CHIU, TSZ K	
20 Church Street			ART UNIT	PAPER NUMBER
22nd Floor			2822	
Hartford, CT 06103				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

usptopatentmail@cantorcolburn.com

Office Action Summary	Application No. 10/501,597	Applicant(s) YU ET AL.
	Examiner Tsz K. Chiu	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 March 2008.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 6-25 is/are pending in the application.

4a) Of the above claim(s) 1-5, 14-19 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 6-13 and 20-25 is/are rejected.

7) Claim(s) 22 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/06/08)
Paper No(s)/Mail Date 0/10/2008

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 6-24 have been considered but are moot in view of the new ground(s) of rejection. This Office Action is response to a Non-final rejection dated: March 10, 2008. The Examiner recognize that claim 6 has been amended, claim 25 newly proposed claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 6-13 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. (5825437) in view of Grace et al. (20020196386) further in view of Nasu et al. (5496752).

With respect to claims 6, 9, 20, 24 and 25, Seo discloses a gate wire (2, For example Fig. 6) formed on an insulating substrate (1, For example Fig. 13) and including a gate line (cross-section taken along line B-B', For example Fig. 6) and a gate electrode (cross-section taken along line A-A', For example Fig. 6) connected to the gate line (cross-section taken along line B-B', For example Fig. 6); a gate insulating film (5, For example Fig. 13) covering the gate wire (2, For example Fig. 6); a semiconductor layer (6, For example Fig. 13) formed on the gate insulating film (5, For

example Fig. 13); a data wire (cross-section taken along line C-C', For example Fig. 6) formed on the gate insulating film (5, For example Fig. 13) or the semiconductor layer (6, For example Fig. 13) and including a data line (3, For example Fig. 13), a source electrode connected to the data line (3, For example Fig. 13) and located on the semiconductor layer (6, For example Fig. 13) and a drain electrode (TFT right reference number 8, For example Fig. 13) formed on the semiconductor layer (6, For example Fig. 13) and located opposite the source electrode (TFT left reference number 8, For example Fig. 13) with respect to the gate electrode (cross-section taken along line A-A', For example Fig. 6); a passivation layer (9, For example Fig. 13) covering the data wire (cross-section taken along line C-C', For example Fig. 6); and a pixel electrode (10, For example Fig. 8e) including a transparent conductive material or a reflective conductive material (ITO or IZO) and connected to the drain electrode (TFT right reference number 8, For example Fig. 13), wherein the gate wire (1 and 2, For example Fig. 6) or the data wire (cross-section taken along line C-C', For example Fig. 6) comprises a metal film (2a, For example Fig. 8e) including a conductive material (column 2, lines 59-65) disposed on the insulating substrate or the gate insulating film (3, For example Fig. 6) and a metal oxide film (4b, For example Fig. 8e) including an oxide of a conductive material.

However Seo does not disclose that the metal oxide is opaque disposed on the metal film.

Grace discloses the back panel of a device may comprise opaque (44, For example Fig. 1) coating on a non-transparent glass disposed on the metal film.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the non-transparent glass of Grace for the purpose of improving the contrast ratio of the display device.

Also Seo does not disclose a side of the metal film is uncovered by the opaque metal oxide film.

Nasu discloses a side of the metal film (50, For example Fig. 38b) is uncovered by the metal oxide film (47, For example Fig. 38a).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the uncovered metal film for the purpose of improving the display quantity.

With respect to claim 7 and 8, Seo discloses wherein the metal film (2a) comprises one of Cr, Mo, Mo alloy, Al and Al alloy and the metal oxide film (4b) comprises one of oxides of Cr, Mo, Mo alloy, Al and Al alloy (column 6, lines 7-12 and 19-24).

With respect to claim 10, Seo discloses wherein the gate wire (1 and 2, For example Fig. 6) further includes a gate pad (2b,3b, For example Fig. 8e) connected to the gate line (cross-section taken along line B-B', For example Fig. 6), and the data wire (cross-section taken along line C-C', For example Fig. 6) further includes a data pad connected to the data line (3, For example Fig. 13), and the thin film transistor array panel further comprises: a subsidiary gate pad (2b,3b, For example Fig. 8e) including substantially the same layer as the pixel electrode (10, For example Fig. 8e) and connected to the gate pad (2b,3b, For example Fig. 8e); and a subsidiary data pad

(2c,3c, For example Fig. 8e) including substantially the same layer as the pixel electrode (10, For example Fig. 8e) connected to the data pad (2c,3c, For example Fig. 8e).

With respect to claim 11, Seo discloses wherein the passivation film (9, For example Fig. 13) comprises SiOC, SiOF, SiNx or an organic insulating material (column 7, lines 55-61).

With respect to claim 12, Seo discloses wherein the semiconductor layer (6, For example Fig. 13) has substantially the same planar shape as the data wire (cross-section taken along line C-C', For example Fig. 6) excluding a channel portion between the source electrode (TFT left reference number 8, For example Fig. 13) and the drain electrode (TFT right reference number 8, For example Fig. 13).

With respect to claim 13, Seo discloses wherein the pixel electrode (10, For example Fig. 8e) is located on the passivation layer (9, For example Fig. 13), and the pixel electrode (10, For example Fig. 8e) and the drain electrode (TFT right reference number 8, For example Fig. 13) are connected to each other via a first contact hole provided in the passivation layer (9, For example Fig. 13).

With respect to claim 20, Seo discloses the metal oxide film (4b, For example Fig. 8e) is formed on a entire top substantially horizontal surface of at least one of the data wire and the gate wire.

With respect to claim 21, Seo discloses a plurality of color filters (column 1, lines 15-20 "...a top plate having color filters...") facing the pixel electrodes, wherein the

plurality of color filters block light (is inherently that color filter block lights since the filter is filtering light).

With respect to claim 23, Seo discloses the gate wire (1 and 2, For example Fig. 6) and the data wire (cross-section taken along line C-C', For example Fig. 6) transmits signals and block light leakage between pixel areas.

With respect to claim 24 Seo discloses drain electrode comprises the metal film (2a, For example Fig. 8e) and the metal oxide film (4b, For example Fig. 8e) and the pixel electrode is connected to the metal film of the drain electrode.

With respect to claim 25, Seo discloses invention set forth to claim 6, however Seo did not disclose the side of the metal film includes opposing sidewalls defining the metal film and the side walls are uncovered by the opaque metal oxide film.

Grace discloses the back panel of a device may comprise opaque (44, For example Fig. 1) coating on a non-transparent glass disposed on the metal film.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the non-transparent glass of Grace for the purpose of improving the contrast ratio of the display device.

Nasu discloses a side of the metal film (50, For example Fig. 38b) is uncovered by the opaque metal oxide film (column 9, lines 35-50).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the uncovered metal oxide film for the purpose of improving the display quantity.

Allowable Subject Matter

Claim 22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 22 is allowable over the reference of record because none of these references disclose or can be combined to yield the claimed invention such as a thin film transistor array panel comprising a plurality of color filters facing the pixel electrodes, wherein the plurality of color filters block light, wherein the portions of adjacent color filters of the plurality of color filters overlap with each other.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art
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TC